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Class	Subclass
ISSUE CLASSIFICATION	

PATENT NUMBER

**6458681**

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## U.S. UTILITY Patent Application

**O.J.P.E.**

PATENT DATE

SCANNED

OCT 01 2002

## APPLICANTS

**TITLE**

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# Methods for providing void-free layers for semiconductor assemblies

PTO-2040  
1259

**ISSUING CLASSIFICATION**

[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b> Sheets Drawg. <u>9</u> Figs. Drawg. <u>37</u> Print Fig. <u>2A</u>			<b>CLAIMS ALLOWED</b> Total Claims <u>18</u> Print Claim for O.G. <u>1</u>	
	<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.  <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____ _____ _____			<b>NOTICE OF ALLOWANCE MAILED</b>  <u>5-16-02</u> <b>ISSUE FEE</b> Amount Due _____    Date Paid <u>08/15/02</u> <sup>63</sup> <u>\$1280.00</u>	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	<b>David Nelms</b> Supervisory Patent Examiner Technology Center 2800 _____ (Primary Examiner) _____ <u>S. Maykey</u> <u>5-200X</u> (Legal Instruments Examiner) (Date)			<b>ISSUE BATCH NUMBER</b>	

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Formal Drawings: \_\_\_\_\_ snts) set \_\_\_\_\_

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